Performance Characterization of Capacitance Modeling for Carbon Nanotube MOSFET

P.Geetha, Dr.R.S.D.Wahida Banu
.

Abstract— Nanostructures performs in a better way with its unique characteristics in the field of electronic devices. Carbon nanotube exhibits 1D electron transport with high mobility because of its density of states for scattering and propagation modes. With the cylindrical electrode structure it possesses good control over the conducting channel. In this paper, CNTMOSFET is modeled for its capacitance and simulated using the CNTMOS tool.

Index Terms—Carbon nanotube, Capacitance Modeling, Energy profile, Electron density, Mobile charge, Density of states, Drive current.

1 INTRODUCTION

CMOS technology plays a vital role in miniaturization of electronic components. The challenges ahead of scaled CMOS with the similar performance of unscaled are

- Physical challenges
- Material challenges
- Power Thermal challenges
- Technological challenges
- Economical Challenges

Decreasing the physical dimension of the device, increases the Tunneling and Leakage current reducing the performance of dielectric material and electrodes. Scaling down increases the density of devices thereby increasing power consumption and thermal dissipation. The techniques used in fabrication of CMOS and to provide resolution below the wavelength of the light become a challenging. Finally, the product should be cost effective besides the production, fabrication and testing cost [6].

Therefore, conventional scaling methods of the device is less effective and other alternative solution is the need for the time. Nanodevices can be a good answer to meet the above challenges. Since the discovery of SWCNT in early '90s, has appreciable application in Electronic, Mechanical and Thermal Properties supporting for new device applications. In CNT the conduction band and valence bands are mirror images of each other unlike silicon. This property supports for designing Complementary devices. [3]

- *P.Geetha is working for Shree Sathyam College of Engineering and Technology,Salem, India. E-mail: pgeetha_me@yahoo.com*
- *R.S.D.Wahida Banu is The Principal, Government College of Engineering,Salem,India.. E-mail: drwahidabanu@gmail.com*

Layers of carbon atoms are arranged in hexagonal lattice called graphite which consists of a two-dimensional sheet of carbon atoms in a honey comb structure. The carbon nanotube is obtained by rolling two-dimensional sheet of carbon atoms.

Nano MOSFETs are needed to be modeled to provide new devices and to know the scaling limits. Modeling explores new device structures with different principles.

There are two different ways of realizing CNTs. They are

- Charge modulation transistor and
- Transmission-Modulation Transistor or Schottky barrier transistor.

The first type is MOSFET-like device in which gate gets charge, supplied from the contacts and the second case is barrier contact and the operation here is by modulating the tunnel barrier width. Here, the first case is taken.[3]

2 STRUCTURE OF CNTMOS

Fig.1 shows the structure of CNTMOS. This model assumes for a cylindrical CNT as the channel and considered CNT as semiconductor. The structure rests on the p^{++} substrate and the remaining structure remains same as that of conventional transistor.

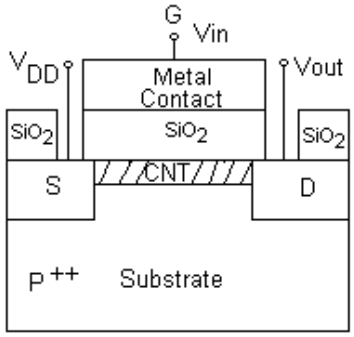


Fig.1. Structure of CNTMOS

3 MODELING OF CNTCMOS

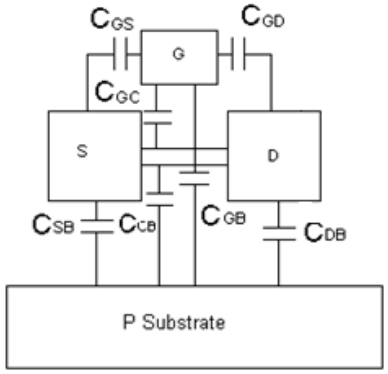


Fig.2. Distribution of Capacitances

The capacitance model of n-type MOS shown in Fig.2. [12]

Where

C_{ox} - C_{GC} - the per unit length electrostatic capacitance between gate and channel,

C_{Sub} - C_{CB} -the per unit length electrostatic capacitance between substrate and channel,

C_{qs} – per unit length quantum capacitance for the channel due to carriers from the source,

C_{qd} – per unit length quantum capacitance for the channel due to carriers from the drain,

C_{gs} – per unit length fringing capacitance between gate and source metal interconnect,

C_{gd} – per unit length fringing capacitance between gate and drain metal interconnect,

$C_{of(g)}$ – C_{gc} – per unit length fringing capacitance between gate and the channel

$C_{of(s)}$ – C_{cb} – per unit length fringing capacitance between gate and the channel

C_{gsub} –electrostatic capacitance between metal and substrate

The model can be approximated as [12]

$$Q_{cap} = C_{ox}(V_G - V_{FB}) + C_{Sub}V_{Sub} + C_c\beta V_{Ch,D} + C_c(1-\beta)V_{Ch,S} - (C_{ox}+C_{Sub}+C_c)\,\Delta\Phi_B/e \quad \text{-- (1)}$$

Where ,

C_c - coupling capacitance between the surface potential and the source,drain.

β - coupling coefficient for the drain.

$1-\beta$ - coupling coefficient for the source

V_{FB} - Flat band voltage

e- Electron charge

$$C_{sub} = 2\pi\kappa\varepsilon_0/(\cosh^{-1}(2H_{Sub}/d)) \text{----------(2)}$$

Where,

κ-dielectric constant of the material

H_{Sub}-oxide thickness

ε_0- dielectric constant of free space

d-diameter of CNT

$$Q_{CNT,S} = 4e/L_x \Sigma\Sigma(1/(1+\exp((E_{m,l} - \Delta\Phi_B)/\kappa T)) \text{ ----------(3)}$$

$$Q_{CNT,D} = 4e/L_x \Sigma\Sigma(1/(1+\exp((E_{m,l} - \Delta\Phi_B + eV_{ch,DS})/\kappa T)) \text{ -----(4)}$$

$$Q_{CNT} = Q_{CNT,S} + Q_{CNT,D} \text{ ----------(5)}$$

$$I_D = 2qk_BT_L/\pi h[f_0(\eta_{F1}) - f_0(\eta_{F2})] \text{----------(8)}$$

Where,

$\eta_{F1} = (E_{F1} - \Delta\Phi_B)/k_BT_L$

$\eta_{F2} = (E_{F2} - \Delta\Phi_B)/k_BT_L$ and

$f_0(\eta_F) = 1/1+\exp((\eta_F - E_f)/k_BT$

$dV_{ch,s}$ and $dV_{ch,D}$ can be found from

$dV_{ch,DS}/dx = I_D/q\mu_n N_{av}A(x)$,

for x=0,

$dV_{ch,s}/dx = I_D/q\mu_n N_{av}A(0)$,

for x=x,

$dV_{ch,D}/dx = I_D/q\mu_n N_{av}A(0)$.

4 SIMULATION

Simulation is done using CNTMOS tool. This model assumes the following parametric values .

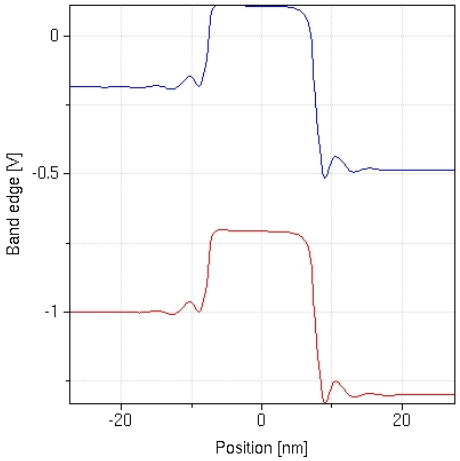
Channel length	=	20nm
Source/drain length	=	10nm
Oxide thickness	=	3nm
Dielectric constant	=	16
CNTdiameter	=	1.7nm
Tight binding parameter	=	3
Gate contact work function	=	0.4084meV
Source/Drain doping	=	$1*10^{\wedge}9/m^2$
Coupling capacitance (Cc)	=	Cox/15
Chirality	=	(16,0)

To study the electrical performance of CNTMOS, an array of seven values for both Vg and Vd are taken for consideration.

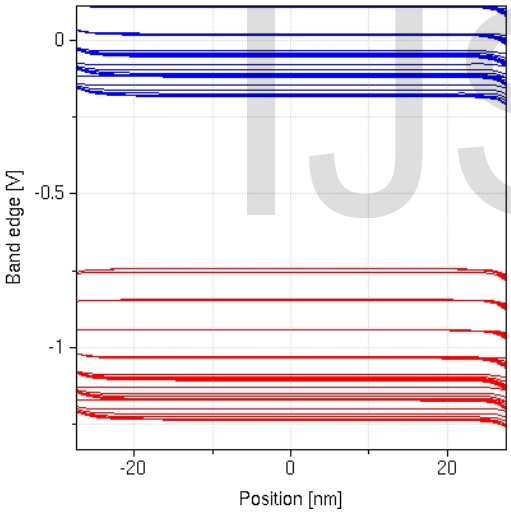
Vg = 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7V

Vd = 0.1, 0.2, 0.3, 0.4, 0.5, 0.6, 0.7V

5 RESULTS AND DISCUSSION

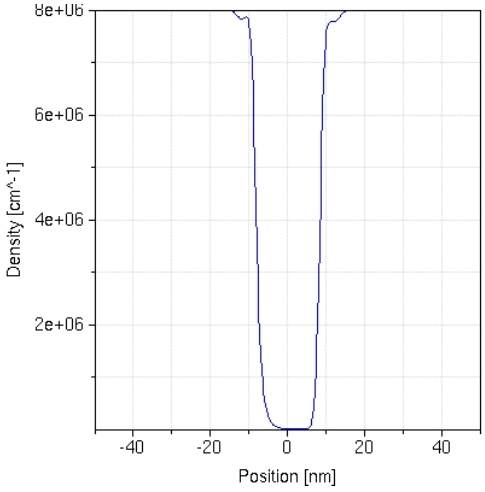


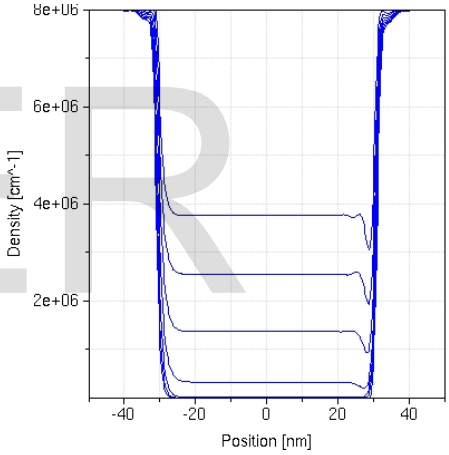
a)



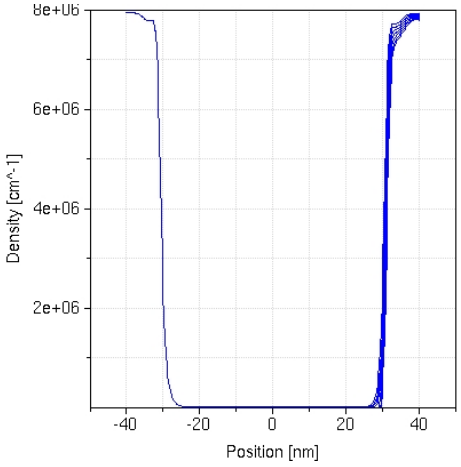
b)

Fig.3.a)&b). Sub band energy profile of CNTMOS for Vg, Vd =0.3V &Vg,Vd =(0.1-1.0)V

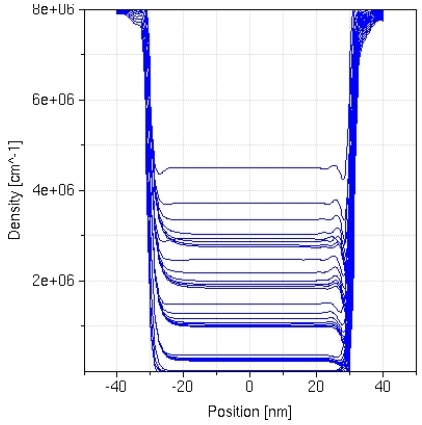




b)



c)



d)

Fig.4. The electron density of first sub band with respect to the gate length for a)Vg,Vd=0.3V b)Vg=(0.1-1.0)V, Vd=0.3 c)Vg=0.3V,Vd=(0.1-1.0)V and d) Vg=(0.1-1.0)V, Vd=(0.1-1.0)V.

The Fig.3. is the subband energy profile for Vg, Vd =0.3V and Vg,Vd =(0.1-1.0)V. From the plots it can be seen that the energy band is rising at the channel region.From the Fig.4 the electron density of the channel is studied. With increase in Vgs and Vds the density gets increase above 4*10^6 per cm also the width is also increasing.

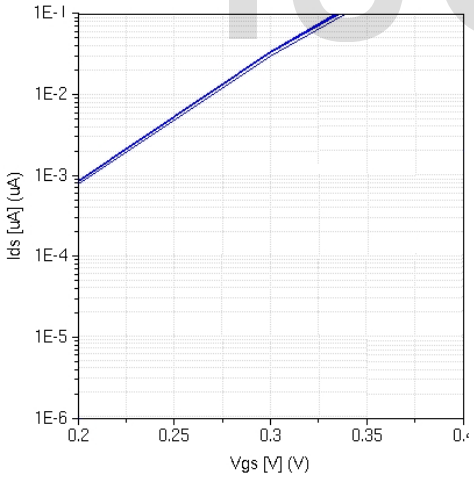


Fig.5. Current of CNTFET relating to gate voltage for Vd=(0.1 -1.0)V

Fig. 5. and Fig.6. projects the relation of current for the gate control voltage and drain voltage. The current increases linearly from 10^{-3}μA to 10^{-1}μA for Vgs and it is above 20μA for Vds greater than 0.8Vand Vgs =1.0V.This rise in current is justified from the above electron density(Fig.4.) and energy profile curves(Fig.3.). That is with higher density and higher energy, more current is flowing. The total mobile charge is piecewise linear and it is steadily increasing for Vg greater than 0.4V.This can be verified from Fig.6, that after Vg=0.4V,the devices enters the saturation region. The memory usage and the time taken (Fig.8)for this simulation gives an idea that the memory usage becomes constant after 150 seconds for around 15MB.Fig.9. is the variation of capacitance for different Vgs. The increment in values of capacitance is due to increase in local density of states in the channel which in turn results in increase in drive current of the device.

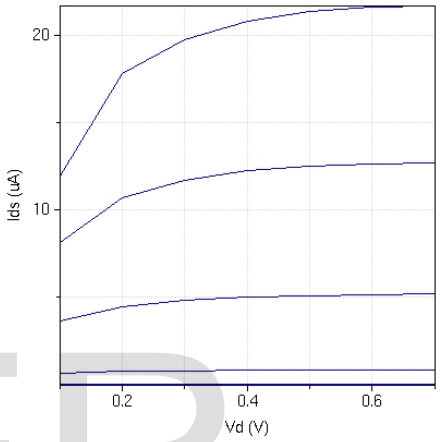


Fig.6.Current Voltage characteristics of CNTMOS for Vgs=0.1V,0.2V,0.8V,1V.

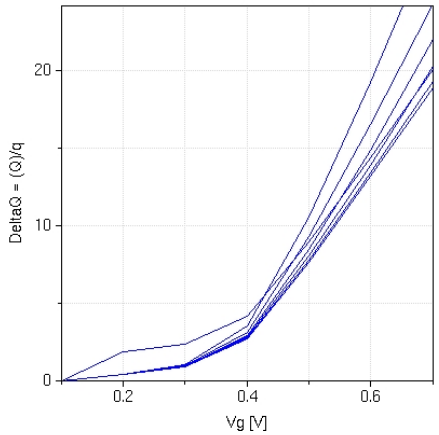
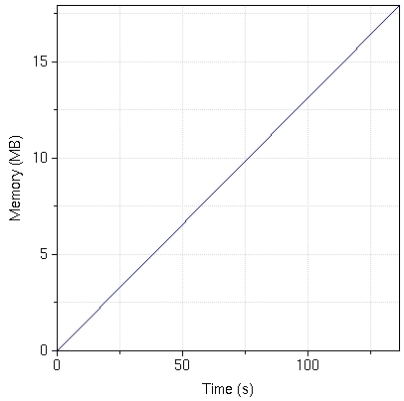
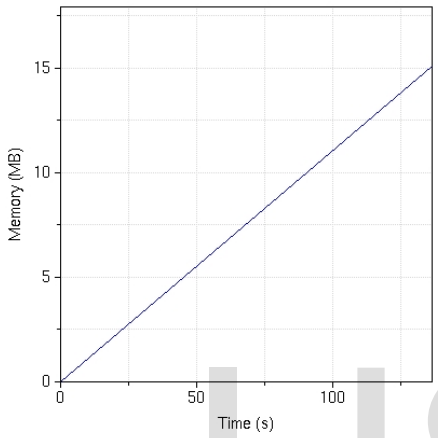


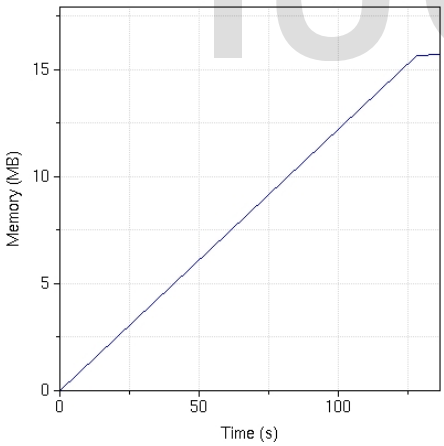
Fig.7. Total mobile charge with respect to gate voltage for various Vd=0.1-1.0V



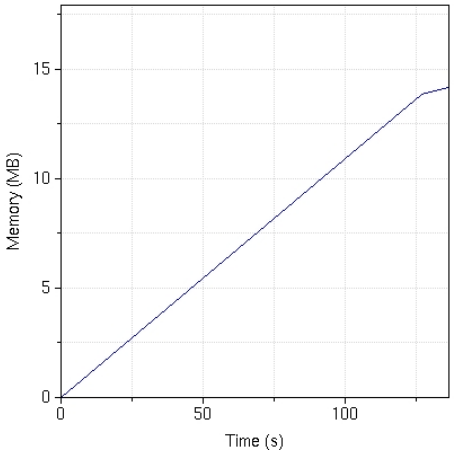
a)



b)

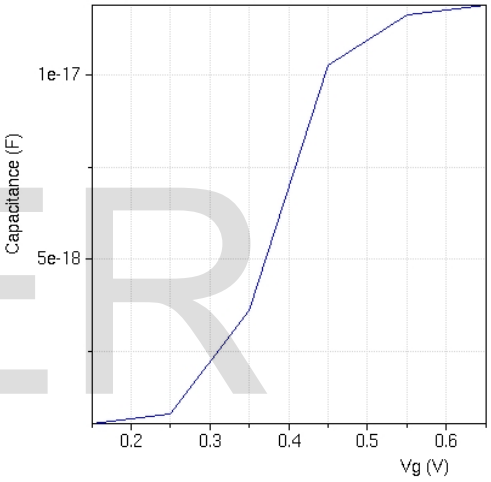


c)

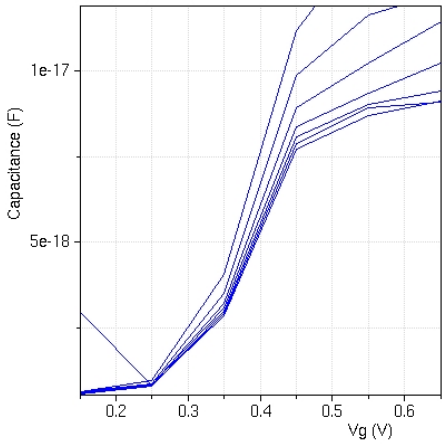


d)

Fig.8.Time taken and the usage of memory for the simulation a)Vg,Vd=0.3V b)Vg=(0.1-1.0)V, Vd=0.3V c)Vg=0.3V,Vd=(0.1-1.0)V and d) Vg=(0.1-1.0)V, Vd=(0.1-1.0)V.



a)



b)

Fig.9.Capacitance for various values of gate control voltage a)Vg=0.3V, Vd=0.3V and

b) Vg=(0.1-1.0)V, Vd=(0.1-1.0)V.

6 CONCLUSION

Carbon nanotube is proving its promising characteristics against the challenges for scaling down the devices size. The transport is ballistic in CNT which makes possible for negligible scattering in propagation of electrons and the length is so short for the accumulation of the energy. This results in more density of electrons and more density of states. The capacitance values increase with the charges and results in increment in current flow. The drive current is 0.4μA[14] for Si whereas it is around 20μaA for ballistic Carbon nanotube MOSFET. In near future it is expected that Carbon nanotube will dominate electronic industry.

REFERENCES

[1] Ben G. Streetman and Sanjay Banerjee," *Solid State Electronic Devices"*,Fifth Edition, Prentice- Hall of India Private Limited.

[2] Riichiro.Satio,G. Dresselhaus and M.S.Dresselhaus " *Physical Properties of Carbon nanotubes"*Imperial College Press, 1998

[3] Mark Lundstrom and Jin Guo, "Nanoscale Transistors-Device Physics, Modeling and simulation*",Springer Science International.*

[4] BanP.Wong,Anurag Mittal,Yu Cao and Greg starr,"Nano –*CMOS Circuit and Physical Design*",Wiley _Inter science, A John Wiley& Sons Inc, Publication.

[5] Changhoo Choi,"Modeling of Nanoscale MOSFETs"*A Dissertation submitted for the doctor of Philosophy,* April 2002.

[6] Nor Zaidi Haron and Said Hamdioii,"Why is CMOS Scaling coming to and End?" Design and test workshop,2008,IDT2008,3rd International.

[7] M.H.Cho,Y.S.Roh,C.N.Whang , Jeong,H.J.Choil,S.W Nam, D.H . Ko,J.H.Lee,N.I.Lee and .Fujihara,"Dielectric Characteristics of Al2O3-HfO2 nanolaminates on Si(100*)",Journal Applied Physics letters,*Volume 81,Number 6,pp.0003-6951/2002/81(6)/1071-1073 Aug 2002.

[8] Kenji Natori,"Compact Modelling of Ballistic Nanowire MOSFETs" *Invited Paper,IEEE Transactions on Electron Devices,*Vol 55 No.11 pp2877-2885,Nov 2008

[9] Anisur Rehman, Jin Guo,Surya Datta and Mark Lundstrom"Theory of Ballistic Transistor", *IEEE Transactions on Electron Devices*,50(9),2003,pp.1853-1864.

[10] E.Ramayya,D.Vasileska,S.M.Goodnick and I,Knezevic,"*Electron transport in Si Nanowires,Journal of Physics* Confernce Series **38**(2006) pp.126-129

[11] Hakon Borl,I,Sigbjorn Kolberg and Tor A.Fjeldy, "Physics based Modeling of Short-Channel nanowire MOSFET" 2008 J. *Phys.: Conf. Ser. 100 052054*

[12] Jun Zh.Huang and Wen-Yan Yin,"Modeling and Performance characterization of Double-Walled Carbon Nanotube Array Field-Effect Transistors", *IEEE Transactions on Electron Devices*,Vol.58,No.1 Jan 2011.

[13] Adel S.Sedra, Kenneth C. Smith," Microelectronic Circuits-Theory and Applications",Fifth Edition, OxfordUniversity Press, New Delhi.

[14] P.Geetha and R.S.D.Wahida banu,"Electrical Characteristics of Carbon Nano Tube and Si-nanowire Metal Oxide Semiconductor FET – A Comparative study", *International Conference on Sustainable Approaches For Green Computing Economy and Environment*,(2013),Salem.